Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **VCL (Logic)**
2. **I OUT**
3. **V –**
4. **I OUT**
5. **BIT 1 (MSB)**
6. **BIT 2**
7. **BIT 3**
8. **BIT 4**
9. **BIT 5**
10. **BIT 6**
11. **BIT 7**
12. **BIT 8**
13. **BIT 9**
14. **BIT 10 (LSB)**
15. **V +**
16. **V REF (+)**
17. **V REF (-)**
18. **COMP**

**.087”**

**12 11 10 9 8 7**

**6**

**5**

**4**

**3**

**2**

**13**

**14**

**15**

**16**

**17 18 1**

**MASK**

**REF**

**6A1**

**1116Z**

**.091”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential:**

**Mask Ref: 1116Z**

**APPROVED BY: DK DIE SIZE .087” X .091” DATE: 8/26/19**

**MFG: ANALOG DEVICES/PMI THICKNESS .020” P/N: DAC10**

**DG 10.1.2**

#### Rev B, 7/1